AMENDMENT TO THE CLAIMS

Please **AMEND** claims 16, 24 and 28; and

Please **ADD** new claim 29 as follows.

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-15 (Canceled).

16. (Currently Amended) A method of fabricating a varactor, comprising:

providing a semiconductor substrate[[:]];

doping a lower region of [[a]] the semiconductor substrate with a first dopant at a first energy level;

doping a middle region of the semiconductor substrate with a second dopant at a second energy level lower than the first energy level; and

doping an upper region of the semiconductor substrate with a third dopant at a third energy level lower than the second energy level.

17. (Original) The method of claim 16, further comprising forming a cathode of a varactor in the lower region, forming a hyper-abrupt junction in the middle region, and forming an anode in the upper region.

18. (Previously Presented) The method of claim 16, further comprising selecting the first dopant from a first N-type dopant, selecting the second dopant from a second N-type dopant, and selecting the third dopant from a P-type dopant.

19. (Original) The method of claim 16, further comprising doping a bottom layer of the lower region of a higher concentration of the first dopant than an upper layer of the lower region.

20. (Previously Presented) The method of claim 19, further comprising forming a collector of the varactor in the upper layer of the lower region of the semiconductor substrate.

21. (Original) The method of claim 16, further comprising forming at least one isolation region adjacent to the lower, middle, and upper regions of the semiconductor substrate.

22. (Original) The method of claim 16, further comprising forming at least one reach-through implant in electrical communication with the lower region of the semiconductor substrate.

23. (Original) The method of claim 16, further comprising forming a silicide layer on a top of the semiconductor substrate above the upper region.

24. (Currently Amended) A method of fabricating a varactor, comprising:

doping a lower region of a substrate layer with a first dopant having a dopant profile such that atoms having a first energy ("A") penetrate to a first depth ("A'") in the substrate layer forming a cathode and atoms having a second energy ("B") penetrate to a second depth ("B'") in the substrate layer forming a collector region above the cathode, wherein [[A>A']] A>B and [[B>B']] A'>B';

doping a middle region of the substrate layer with a second dopant, the middle region being tailored for an implant profile that forms an anode, the second dopant overlapping the collector region; and

doping an upper region of the substrate layer with a source/drain type implant to form the anode,

wherein the doping of the middle region has approximately less energy than the doping of the lower region and the doping of the upper region has approximately less energy than the doping of the middle region.

25. (Previously Presented) The method of claim 24, wherein the forming of the collector region and the cathode are formed in a single doping step via energy distribution of a single dopant type.

26. (Previously Presented) The method of claim 24, wherein an active portion of the varactor is formed in a column from the substrate layer which is a semiconductor material.

27. (Previously Presented) The method of claim 16, wherein the second dopant is deposited at a shallower depth than the first dopant and the third dopant is deposited at a shallower depth than the second.

28. (Currently Amended) The method of claim 16, wherein only three doping steps [[a-c]] are utilized to form the varactor with a cathode, a collector, an HA junction, and an anode.

29. (New) A method of fabricating a varactor, comprising:

forming a semiconductor substrate;

doping a lower region of the semiconductor substrate with a first dopant at a first energy level;

doping a middle region of the semiconductor substrate with a second dopant at a second energy level lower than the first energy level; and

doping an upper region of the semiconductor substrate with a third dopant at a third energy level lower than the second energy level,

wherein the semiconductor substrate includes a collector region and a cathode that are formed in a single doping step via energy distribution of a single dopant type.